SESSION 22 – TAPA I
Advanced CMOS Technology II

Thursday, June 17, 3:25 p.m.
Chairpersons: S. Sharifzadeh, Cypress Semiconductor
T. Nakamura, Rohm

22.1 — 3:25 p.m.
The Revolutionary and Truly 3-Deminsional 25F^2 SRAM Technology with the Smallest S^3 (Stacked Single-Crystal Si) Cell, 0.16μm^2, and SSTFT (Staced Single-Crystal Thin Film Transistor) for Ultra High Density SRAM, S.-M. Jung, J. Jang, W. Cho, J. Moon, K. Kwak, B. Choi, B. Hwang, H. Lim, J. Jeong, J. Kim and K. Kim, Samsung Electronics, Kyungki-do, Korea

The smallest 25F^2 SRAM cell size of 0.16 um^2 is realized by S^3 cell technology and SSTFT with 193nm ArF lithography process. The stacked single-crystal thin film is developed and used *for the first time* in the SRAM cell to make the SRAM products comparative to the DRAM products in the density and the cost. The load PMOS and pass NMOS transistors are stacked over the planar pull-down NMOS transistors to drastically reduce the cell size. In this study, the dream of truly 3D memory device is achieved by fabricating 64M bit density SRAM.

22.2 — 3:50 p.m.
A CPU on a Plastic Film Substrate, T. Takayama, Y. Ohno, Y. Goto, A. Machida, M. Fujita, J. Maruyama, K. Kato, J. Koyama and S. Yamazaki, Semiconductor Energy Laboratory Co., Ltd., Kanagawa, Japan

A CPU using a high performance poly-silicon TFT is successfully fabricated on a plastic film substrate by a TFT transfer technology onto a plastic film substrate we developed. No performance degradation by the transfer process was observed, and we confirmed the CPU operation at the frequency of more than 10MHz with a power source voltage 3.3V.

22.3 — 4:15 p.m.
Soft Error Free, Low Power and Low Cost superSRAM with 0.98μm^2 Cell By Utilizing Existing 0.15μm-DRAM Process, Y. Fujii, Y. Ishigaki, T. Hosokawa, M. Dei, Y. Maki, A. Nishida, T. Izutsu, Y. Nakashima, R. Toyota, T. Koga, T. Ipposhi, Y. Konishi and Y. Kihara, Renesas Technology Corp., Hyogo, Japan

16M-superSRAM with 0.98um2 is developed by existing 0.15um DRAM processes. As a result, the standby current and random access time of fabricated 16M-superSRAM are about 0.2uA/chip and 43ns at RT. As super SRAM has a cylindrical stacked capacitor at each node, very high tolerance for SER (soft error rate) is expected as compared with conventional 6Tr-SRAMs. By alpha ray irradiated experiments, an SER free feature of superSRAM is confirmed for the first time.

22.4 — 4:40 p.m.
A New Vertically Stacked Poly-Si MOSFET with Partially Depleted SOI Operation for Densely Integrated SoC Applications, H. Matsuoka, T. Mine, K. Nakazato*, M. Moniwa**, Y. Takahashi**, M. Matsuoka**, H. Chakihara**, A. Fujimoto** and K. Okuyama**, Hitachi Ltd., Tokyo, Japan, *Hitachi Europe, Ltd., Cambridge, UK, **Renesas Technology Corp., Tokyo, Japan

We have described a vertical poly-Si MOSFET for densely integrated SoC applications. Through low-temperature solid-phase growth, we successfully obtained large grains and thus excellent DC characteristics. Furthermore, partially depleted SOI operation suppresses variation in threshold voltage to the same levels as are seen with bulk pMOS devices. The effect of this vertical device in application to 6T-SRAM was significant, since we confirmed effective operation and realized state-of-the-art (90-nm-process) cell size with one-generation-earlier (0.13-um) technology.